UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/521,955	08/17/2005	Craig J. Boucher	EBA-0022	2081

23413 7590 02/01/2008

CANTOR COLBURN, LLP
20 Church Street
22nd Floor
Hartford, CT 06103

EXAMINER	
KITOV, ZEEV V	
ART UNIT	**PAPER NUMBER**
2836	

MAIL DATE	DELIVERY MODE
02/01/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/521,955	BOUCHER, CRAIG J.	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Examiner acknowledges a submission of the arguments filed on November 20, 2007. A new Office Action follows.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1- 5, 7, 9, 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aikow et al. (US 4,712,477) in view of Miller et al. (US 5,946,177). Regarding Claim 1, Aikow et al. disclose an initiator (16 in Fig. 6) having signal input nodes. It further discloses a timer portion (8 and 9 in Fig. 6) connected to the input nodes (10 and 11 in Fig. 6) and to initiator (16 in Fig. 6). The timer serves as a protective circuitry protecting the initiator from being activated by occasional short pulse on the power lines. The timer further issuing a release signal to the initiator, i.e. after receipt of the input signal and after passage of its timing interval the timer activates the initiator.

However, it does not disclose a protective circuitry with a clamping portion capable of protecting the initiator against powerful short pulses, such as ESD events. Miller discloses the ESD protection circuitry (Fig. 1) connected across the input signal

nodes (Vdd and Vss in Fig. 1) responsive to signals at the input nodes (presence of a voltage in the input nodes) with a clamping portion (25 in Fig. 1), which is triggered into clamping action by the timer, i.e. RC triggering circuit (30 and 35 in Fig. 1) by diverting at least portion of the input signal from a protected load. The timer of Miller circuit (15 in Fig. 1) is connected to the clamping portion (20 and 25 in Fig. 1) and to the input nodes and being responsive to the input signals (appearance of the voltage on the power supply nodes; after receipt of the input signal (appearance of the voltage on the power sup[ply lines) followed by passage of clamping interval (defined by RC time constant) the timer issues a release signal to the clamping portion (shown in Fig. 5).

The RC timer circuit of Miller is an exact copy of the RC element of Aikow et al. Moreover, both timers use the same input signals. The only difference is in connection of their outputs; the output of Aikow timer after passage of delay time provides a voltage to an initiator, while the Miller timer after passage of delay time stops the clamping action provides a voltage to the load. Therefore, due to absolute identity of the schematic structure including the input and output connection and a way of functioning, of the timers the designer considering their combination would inevitably eliminate the redundancy and use a single timer rather than two. Such minimization does not represent the invention but rather normal in the design attempt to exclude the redundancy and to minimize amount of structurally and functionally identical pieces of equipment.

When the circuits are combined together the same timer of Aikow, which activates the initiator is used as a timer for timing the clamping action of the clamping

transistor. The clamping transistor of Miller is connected across a protected element, i.e., in the Aikow circuit modified according to teachings of Miller, the clamping transistor is connected across the initiator. In such circuit when the input signal lasts longer than the time necessary to fully charge capacitor (35 in Fig. 1 of Miller) in the triggering circuit, the clamping transistor is switched back to non-conductance (as shown in Fig. 5 of Miller) and therefore, the clamping portion being responsive to a release signal (presence of voltage on the power supply lines lasting long enough time) to permit the input signal to pass to the initiation element (16 in Fig. 6 of Aikow) upon receipt of such release signal.

In such circuit a timer portion is being connected to the clamping portion, i.e. to the clamping transistor and additionally both the timer and clamping circuit use the same input (voltage on power supply lines). In such circuit the timer is being responsive to input signals (voltage on the power supply lines), after passage of a clamping interval the timer issuing a release signal to the clamping portion after the receipt of the input signal, i.e. presence of the voltage on the power supply lines after clamping interval causes the timer to activate the initiator.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the ESD protection arrangement of Miller to the Aikow circuit and was stated above to combine two identical timers into a single timer, because such circuit as all other electronic circuits need the ESD protection since as well known in the art electrostatic discharge, for example from humans, may inadvertently activate the initiator.

Regarding Claims 2 – 4, Aikow et al. disclose the timing interval being selected from fraction of millisecond to several milliseconds (col. 6, lines 9 – 16). Duration of timing interval should be selected such to activate the clamp in a case of real ESD event and to ignore some spurious not dangerous voltage deviations. Therefore, the time delay duration presents a result effective variable, which may be optimized by experimenting. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Baginski solution by setting the time delay to some specific value, because as Court Decision *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955) states: "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."

Regarding Claim 5, Miller et al. disclose a unipolar clamping circuit (25 and 20 in Fig. 1) and unipolar timer circuit (15 in Fig. 1). According to The Authoritative Dictionary of IEEE Standard Terms, the unipolar transistor is "a transistor that utilizes charge carriers of only one polarity". Therefore, the MOSFET is a proper unipolar transistor.

Regarding Claim 7, Aikow et al. disclose the electronic delay detonator built as monolithic IC (Fig. 1) and Miller et al. disclose the ESD protection circuit used for protection of integrated circuits and therefore being a part of the integrated circuit (col. 1, lines 11 – 14).

Regarding Claim 9, in the Aikow et al. system modified according to teachings of Miller et al. the clamping portion (25 in Fig. 1 of Miller) is responsive to an input signal (appearance of the voltage on the power supply lines) to divert a portion of the input

signal by drawing the current through the clamping portion when the signal is about the threshold (the threshold is set by an input of the CMOS inverter (20 in Fig. 1 of Miller) while permitting a second none-zero portion of the input signal (continuation of presence of the power supply voltage) to pass to the protected load (initiator 16 in Fig. 1 of Aikow). A motivation for modification of the primary reference is the same as above.

As per Claim 10, requiring the input signal lasting longer than a sum of the clamping interval and the function time of the initiator, it is routine decision of the designer based on his knowledge of explosion initiation process and application of a common sense. It is clear that if the input signal does not last long enough to bypass the clamping action and to let initiator to ignite the explosive charge, the system will fail. It would be obvious to one of ordinary skill in the art at the time the invention was made to provide the input signal sufficient for bypassing the clamping action and letting the initiator to ignite the explosive charge, since such decision is in accordance a basic rule of ordinance explosion technique with application of common sense.

Regarding Claim 12, In the Aikow et al. system modified according to teachings of Miller et al. the clamping portion is electrically connected in parallel with the input nodes of the initiation element (see Claim 1 rejection above).

Claims 8 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aikow et al. in view of Miller et al. and Baginski (US 6,192,802). As per Claim 8, it differs from Claims 1 and 7 rejected above by its limitation of some structural details of mounting the initiation element and the protective element. Baginski discloses an

electro-explosive device protected against ESD having the initiative element and protective circuit being mounted on a header (62 in Fig. 6) with two electrical leads (66 and 66' in Fig. 6) connected to the protective circuit (Fig. 11A and 12A) and further including a shell (68 in Fig. 6) mounted on the header and a charge of reactive material (69 in Fig. 6) in the shell. It would have been obvious to one of ordinary skill in the art at the time the invention was made to mount the initiator element of the explosive device together with the a charge of reactive material in the shell mounted on the header according to teachings of Baginski, because (a) the charge of reactive material which should be located together with the initiator must have a good isolation from an environment and (b) because such mounting was recognized as part of the ordinary capabilities of one skilled in the art.

As per Claim 11, it requires the time interval of the clamping portion being smaller than duration of the proper initiation signal. According to Miller et al. (see Fig. 5) the clamping interval lasts no longer than 300 nanoseconds, while according to Aikow et al. (col. 6, lines 1 – 16), the detonator ignition element is ignited with a present delay time from 10 to several hundreds milliseconds. It is clear that combined circuit with timer setting of Miller satisfies requirements of Claim 11. As to permitting an adequate portion of the proper initiation signal (remainder of the input signal after end of clamping) to pass to the initiation element, it is normal requirement for blasting the explosive charge. It would have been obvious to one of ordinary skill in the art at the time the invention was made to set the clamping time such that it would be able to suppress the ESD event wile permitting the remainder of the input signal to have

sufficient duration for initiating the explosion, as demonstrated by Baginski, which suppresses the short ESD pulses by filtering them out and letting the longer lasting signals to pass to initiator, such technique was recognized as part of the ordinary capabilities of one skilled in the art.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aikow et al. in view of Miller et al. and Avery et al. (US 6,501,632). Claim 6 differs from Claim 1 rejected above by its limitation of using bipolar transistors. Avery et al. disclose the ESD protection circuit having the clamp portion formed by NMOS transistor with parasitic NPN transistor (in Fig. 3) and the timer portion formed by zener diodes (Z1, Z2 in Fig. 34) and parasitic zener diode resistance (Rz1 in Fig. 3). Both the clamp and the timer circuits are based on bipolar junction technology. The reference has the same problem solving area, namely providing ESD protection for the semiconductor circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Aikow et al. solution by replacing the MOSFET elements by their bipolar junction equivalents according to teachings of Avery et al., because such solution has a number of advantages, such as: (I) the MOSFET/NPN clamp has an advantage of being extremely sensitive as MOSFET to the gate voltage (practically no current is necessary) and at the same time being able to withstand higher values of voltages and currents than MOSFET; (II) the zener diodes biasing and timing circuit according to Avery et al. (col. 3, lines 20 – 35), has an advantage of enabling the nMOS transistor to be biased to optimum conditions for bipolar snapback.

Response to Arguments

Applicant's arguments have been fully considered but they are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry, can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (571) 273-8300 for all communications.

Z.K.
1/25/2008

1/30/08

MICHAEL SHERRY
SUPERVISORY PATENT EXAMINER